REMARKS

Claim Rejections 35 U.S.C. § 103 (a)

The Examiner has rejected claims 31-39 under 35 U.S.C. §103 (a) as being unpatentable over Efland et al. (US 6,025,275) and Byrne (US 5,136,364) in view of Yabu et al. (US 5,989,992).

Applicant respectfully disagrees with the Examiner. Applicant has amended claim 31 and added new claims 55-62. Applicant submits that the three references cited by the Examiner do not teach, suggest, or render obvious the method of Applicant's invention as claimed in claims 31-39 and 55-62.

Claim 31, as amended, of Applicant's claimed invention discloses a method including: providing a substrate (300); forming a metal layer over the substrate, the metal layer including a bond pad (304) and a first member (306), the bond pad and the first member being separated by a gap (308); forming a first material (310) over the bond pad and over the first member, the first material having a low dielectric constant, the first material having a thickness to fill the gap; forming a second material (312) over the first material, the second material being thin and resistant to moisture penetration, the second material being kept above the bond pad and the first member and out of the gap; forming a third material (314) over the second material; forming an opening (316) with tapered sidewalls in said third material and vertical sidewalls in said second material and said first material to expose a top surface of said bond pad; forming a fourth material (318) over the third material, the tapered and vertical sidewalls of the opening, and the top surface of the bond pad, the fourth material being conductive, the fourth material having a thickness to prevent moisture penetration; and forming a bump (320) on the fourth material over the sidewalls of the opening and over the top surface of the bond pad. See Figures 3a - 3h. Also, see pages 8-14 of the specification.

In contrast, Efland et al. teaches a method of forming a thick plated interconnect (80) for a semiconductor device that includes: forming a metal layer (20) above a semiconductor layer (12); forming a dielectric layer (22) on the metal layer; forming a via (24) in the dielectric layer to expose the metal layer; forming a copper lead (50) that is electrically coupled to the metal layer through the via of the dielectric layer; forming a barrier member (88) on the copper lead; and forming a bondable layer (86) comprising aluminum on the barrier member. See Figures 1A – 1E.

Furthermore, Byrne teaches a bonding pad structure for a die that includes: a substrate (10); a bonding pad (11) on the substrate; a passivation layer (12) on the substrate and the bonding pad; a hole in the passivation layer to expose the center portion of the bonding pad; three metal layers: an aluminum layer (14), a barrier metal layer (15), and a noble metal layer (15), to cover the hole; and an additional passivation layer (17) to seal the edges of the three metal layers (14, 15, 16) to exclude potential moisture and ionic contaminants which may promote corrosion. See Figure 3.

In addition, Yabu et al. teaches a method of manufacturing a semiconductor device that includes: forming an interlayer insulating film (11) on a semiconductor substrate; forming metal wires (12) and a bonding pad (15) on the interlayer insulating film; forming a surface protecting film (20) to cover the interlayer insulating film and the metal wires, the surface protecting film being a composite film that includes a buried insulating film (13) with a small dielectric constant and a passivation film (14) of an insulating film with a large dielectric constant and high moisture absorption resistance; forming an opening (20a) in the surface protecting film in an area for forming a bonding pad; depositing a metal film (15x) to fill the opening and extend over the passivation film; and patterning the metal film to form the bonding pad. See Figures 2(a)-2(d) and Figure 1.

However, none of the three cited references teaches forming an opening with tapered sidewalls in a third material and vertical sidewalls in underlying second material and first material to expose a top surface of a bond pad, where the first

material has a low dielectric constant and the second material is thin and resistant to moisture penetration. On the contrary, all three cited references teach an opening with vertical sidewalls. Vertical sidewalls may be formed with an anisotropic process while tapered sidewalls may be formed with an isotropic process.

Thus, combination of the methods of the three references, Efland et al., Byrne, and Yabu et al., cited by the Examiner will not produce the method of Applicant's invention as claimed in claim 31 so Applicant submits that the three references cited by the Examiner do not teach, suggest, or render obvious the method of Applicant's invention, as claimed in claim 31, to one of ordinary skill in the art of manufacturing semiconductors at the time the invention was made.

Claims 32-39 are dependent on claim 31. Thus, combination of the methods of the three references, Efland et al., Byrne, and Yabu et al., cited by the Examiner will also not produce the method of Applicant's invention as claimed in claims 33-39 so Applicant also submits that the three references cited by the Examiner also do not teach, suggest, or render obvious the method of Applicant's invention, as claimed in claims 32-39, to one of ordinary skill in the art of manufacturing semiconductors at the time the invention was made.

In view of the foregoing, Applicant respectfully requests the Examiner to withdraw the rejections to independent claim 31 and dependent claims 32-39 under 35 U.S.C. §103 (a).

Applicant believes that all claims pending, including amended claim 31, claims 32-39, and new claims 55-62, are now in condition for allowance so such action is earnestly solicited at the earliest possible date.

PETITION FOR EXTENSION OF TIME PURSUANT TO 37 C.F.R. § 1.136 (a)

Applicant respectfully petitions pursuant to 37 CFR 1.136(a) for a three-month extension of time to file this response to the Office Action mailed April 8, 2004. The extended period is set to expire on Friday, October 8, 2004. A check in the amount of $950.00 is enclosed to cover the fee for a three-month extension of time.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time.

Should there be any additional charge or fee, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, please charge Deposit Account No. 02-2666.

If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact the undersigned at (408) 720-8300.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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